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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,964	INUKAI, KAZUTAKA	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-34* is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-12-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment with the request for continuation examination filed December 12, 2005 is entered and claims 2-34 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 2-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 2, 3, 10, 21, and 22 are rejected under 35 USC 102 (e) as being unpatentable over US Patent Application # 20020044124 ("Yamazaki et al.").

As per claim 2, Yamazaki et al. teach a display device comprising a plurality of pixels arranged in a pixel portion (the pixel structure of the EL display device in accordance with the present invention will be described with reference to FIG. 16 (page 15, paragraph 0232),

a plurality of pixels arranged in each pixel column and two or more data lines extend in each of the pixels to simultaneously supply video signals to the pixels though the data lines (a plurality of pixels 104 are arranged in each pixel column coming from the row driver (102), two or more data lines extend in each of the pixels coming from the data driver (101) to simultaneously supply video signals to the pixels though the data lines (see Fig.1).

As per claim 3, Yamazaki et al. teach a pixel portion Fig.5 (103) comprising a switching element (201) and EL element (204) corresponding to wherein the pixels each have a switching element and a light emitting element, and wherein the switching element is connected to one of the two or more data lines, which is predetermined for each pixel.

As per claim 10, Yamazaki et al. teach the EL display device is also referred to as organic EL display (OELD) or an organic light emitting diode (OLED) (page 1, lines 0006)corresponding to wherein the light emitting element comprises an OLED.

As for claim 21, Yamazaki et al. teach a display device (the pixel structure of the EL display device in accordance with the present invention will be described with reference to FIG. 16 (page 15, paragraph 0232) comprising:

a plurality of data lines (a data driver Fig.1 (101) where a plurality of data lines are from the extend over the pixel portion (103);

a plurality of scanning lines (a row driver Fig.1 (102) where a plurality of scanning lines are from the extend over the pixel portion (103);

a plurality of pixels arranged in rows and columns (pixel (104) in the pixel portion Fig.1 (103));

at least first and second pixel electrodes arranged in one of the columns (the EL element 204 is connected to the drain region of the EL driver TFT 202, then the anode of the EL element 204 becomes the opposing electrode, and the cathode becomes the pixel electrode, and it is preferable that an n-channel TFT be used as the EL driver TFT 202 (page 6, paragraph 0105));

a first data line operationally connected to the first pixel electrode (the EL element 507 is connected to the drain region of the EL driver TFT 504, then the anode of the EL element 507 becomes the pixel electrode and a cathode becomes the opposing electrode, and it is preferable that the EL driver TFT 504 be formed using a p-channel TFT. Conversely, if the cathode of the EL element 507 is connected to the drain region of the EL driver TFT 504, the anode of the EL element 507 becomes the opposing electrode, and the cathode becomes the pixel electrode, and it is preferable that the EL driver TFT 504 be formed using an n-channel TFT (page 9, paragraph 0146));

a second data line operationally connected to the second pixel electrode (the EL element 507 is connected to the drain region of the EL driver TFT 504, then the anode of the EL element 507 becomes the pixel electrode and a cathode becomes the opposing electrode, and it is preferable that the EL driver TFT 504 be formed using a p-channel TFT. Conversely, if the cathode of the EL element 507 is connected to the drain region of the EL driver TFT 504, the anode of the EL element 507 becomes the

opposing electrode, and the cathode becomes the pixel electrode, and it is preferable that the EL driver TFT 504 be formed using an n-channel TFT (page 9, paragraph 0146));

a first scanning line of the plurality of scanning lines intersecting with the first data line (see Fig.1, the pixel (104) where the data lines and scanning lines are intersecting;

a second scanning line of the plurality of scanning lines intersecting with the second data line (see Fig.1, the pixel (104) where the data lines and scanning lines are intersecting; and

wherein the pixels each a light-emitting element (EL element Fig.5 (204)).

As for claim 22, Yamazaki et al. teach the light emitting element comprises an OLED (EL elements as self-light emitting elements has become spirited. The EL display device is also referred to as organic EL display (OELD) or an organic light emitting diode (OLED) (page 1, paragraph 0006)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-9 and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application # 20020044124 ("Yamazaki et al.") in view of US Patent # 5,999,154 ("Yoshioka").

As per claim 4, Yamazaki et al. teach a display device (the pixel structure of the EL display device in accordance with the present invention will be described with reference to FIG. 16 (page 15, paragraph 0232) comprising:

a plurality of pixels arranged in a matrix pattern in a pixel portion Fig.1 (103), the matrix pattern having a plurality of pixel columns in which the pixels are arranged in a column direction (a plurality pf pixel columns coming from the row driver Fig.1 (102) to extend across all the pixels in the pixel portion (103);

a plurality of data lines extending in a column direction (a plurality of data signal lines coming from the data driver (101) to extend across all the pixels in the pixel portion (103));

a plurality of scanning lines extending in a row direction (a plurality of column signal lines coming from the row driver (102) to extend across all the pixels in the display portion (103)),

a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding a plurality of pixels arranged into a matrix pattern, the pixels each having a light emitting element (204),

wherein the pixels each having a light emitting element (EL element Fig.5 (204));

wherein x data lines (x is a natural number equal to or larger than 4) out of the plurality of the data lines extend in each of the pixel columns and one scanning line out

of the plural scanning lines in each row (see in Fig.1, a plurality of data lines coming from the data driver (101) that extend across all the pixels in the pixel portion and a plurality of scanning lines coming from the row driver (102) that extend across all the pixel in the pixel portion. Accordingly, the prior art teach all the claimed limitations with the exception of providing y scanning drivers (y is a natural number equal to or larger than 1) are provided to select x scanning lines out of the plural scanning lines simultaneously, and wherein x data drivers are provided to simultaneously supply signals to x pixels selected out of the plurality of pixels through the x data lines in each of the pixel columns.

However, Yashioka teaches the display unit 10' has 1000 scanning lines, and these scanning lines are divided into, for example, eight groups A to H. Hence, in each of the groups A to H, the scanning line is selected simultaneously, so that different data can be written simultaneously into the groups A to H (column 11, lines 34-39)).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the display selection as taught by Yoshioka in the display panel disclosed by Yamazaki because this would provide an image display method capable of enhancing the rate of period contributing to display within the period of one field, and obtaining a bright display image, and a device used in execution thereof (column 3, lines 19-23).

As per claim 5, Yamazaki et al. teach a display device (the pixel structure of the EL display device in accordance with the present invention will be described with reference to FIG. 16 (page 15, paragraph 0232) comprising:

a plurality of pixels arranged in a matrix pattern in a pixel portion Fig.1 (103), the matrix pattern having a plurality of pixel columns in which the pixels are arranged in a column direction (a plurality pf pixel columns coming from the row driver Fig.1 (102) to extend across all the pixels in the pixel portion (103);

x data lines (x is a natural number equal to or larger than 2) placed in each pixel column (data lines coming from the data driver Fig.1 (101) where 2 data lines are extending across pixel 104 in the pixel portion (103);

one scanning line placed in each row (one scanning line from the row driver Fig.1 (102); and

a plurality of pixels placed at points where the data lines and the scanning line intersect to form a matrix pattern, the pixels each having a light emitting element (204).

Accordingly, the prior art teach all the claimed limitations with the exception of providing wherein y scanning drivers (y is a natural number equal to or larger than 1) are provided to select x scanning lines out of the plural scanning lines simultaneously, and wherein x data drivers are provided to simultaneously supply signals to x pixels selected out of the plural pixels through the x data lines placed in each column.

However, Yashioka teaches the display unit 10' has 1000 scanning lines, and these scanning lines are divided into, for example, eight groups A to H. Hence, in each of the groups A to H, the scanning line is selected simultaneously, so that different data can be written simultaneously into the groups A to H (column 11, lines 34-39)).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the display selection as taught by Yoshioka in

the display panel disclosed by Yamazaki because this would provide an image display method capable of enhancing the rate of period contributing to display within the period of one field, and obtaining a bright display image, and a device used in execution thereof (column 3, lines 19-23).

As to claim 6, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register, a buffer, a level shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to the x data drivers each have a plurality of shift registers and sampling circuits and the shift registers each operating independently, each of the sampling circuits being associated with one of the shift registers.

As to claim 7, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register, a buffer, a level shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to the x data drivers each have a plurality of shift registers and sampling circuits and the shift registers each operating independently, each of the sampling circuits being associated with one of the shift registers.

As to claim 8, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register (first and second latches), a buffer, a level shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to wherein the x data drivers each have a plurality of shift registers, first latches, second latches, and sampling circuits, the shift registers each operating independently, each of the first latches, each of the second latches, and each of the sampling circuits being associated with one of the shift registers.

As to claim 9, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register (first and second latches), a buffer, a level shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to wherein the x data drivers each have a plurality of shift registers, first latches, second latches, and sampling circuits, the shift registers each operating independently, each of the first latches, each of the second latches, and each of the sampling circuits being associated with one of the shift registers.

As per claim 11, Yamazaki et al. teach the EL display device is also referred to as organic EL display (OELD) or an organic light emitting diode (OLED) (page 1, lines 0006)corresponding to wherein the light emitting element comprises an OLED.

As per claim 12, Yamazaki et al. teach the EL display device is also referred to as organic EL display (OELD) or an organic light emitting diode (OLED) (page 1, lines 0006)corresponding to wherein the light emitting element comprises an OLED.

As to claim 13 , Yamazaki et al. teach a source signal line driver circuit Fig.1 (101) and a gate signal line driver circuit (102) are formed on the same conductive film 105 formed on the pixel portion 103 corresponding to wherein the plural pixels, the y scanning drivers, and the x data drivers are formed on the same insulator.

As to claim 14, Yamazaki et al. teach a source signal line driver circuit Fig.1 (101) and a gate signal line driver circuit (102) are formed on the same conductive film 105 formed on the pixel portion 103 corresponding to wherein the plural pixels, the y scanning drivers, and the x data drivers are formed on the same insulator.

As per claims 15, Yamazaki et al. teach a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to wherein the pixels each have a driving transistor Fig.5 (202), a switching transistor (201), and a capacitor (203), the driving transistor (202) controlling a current value of the light emitting element (204), the switching transistor (201)controlling input of a video signal into its pixel, and the capacitor (203) holding the video signal and the erasing transistor Fig.6 (504) discharging electric charges that are held in the capacitor.

As per claim 16, Yamazaki et al. teach a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to wherein the pixels each have a driving transistor Fig.5 (202), a switching transistor (201), and a capacitor (203), the driving transistor (202) controlling a current value of the light emitting element (204), the switching transistor (201)controlling input of a video signal into its pixel, and the capacitor (203) holding the video signal and the erasing transistor Fig.6 (504) discharging electric charges that are held in the capacitor.

As per claim 17, Yamazaki et al. teach a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to wherein the pixels each have a driving transistor Fig.5 (202), a switching transistor (201), and a capacitor (203), the driving transistor (202) controlling a current value of the light emitting element (204), the switching transistor (201)controlling input of a video signal into its pixel, and the capacitor (203) holding the video signal and the erasing transistor Fig.6 (504) discharging electric charges that are held in the capacitor.

As per claim 18, Yamazaki et al. teach a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to wherein the pixels each have a driving transistor Fig.5 (202), a switching transistor (201), and a capacitor (203), the driving transistor (202) controlling a current value of the light emitting element (204), the switching transistor (201)controlling input of a video signal into its pixel, and the capacitor (203) holding the video signal and the erasing transistor Fig.6 (504) discharging electric charges that are held in the capacitor.

5. Claims 19 and 20 are rejected under 35 USC 103 (e) as being unpatentable over US Patent Application # 20010035863 ("Kimura") in view of US Patent # 5,999,154 ("Yoshioki").

As for claim 19, Kimura et al. teach a driving method of a display device (an active EL display device is shown in FIGS. 13A and 13B. FIG. 13A is a schematic diagram of an entire circuit) that has a plurality of pixels arranged in a matrix pattern in a pixel portion (pixel Fig.3A (300) is arranged in a pixel matrix 351) , the matrix pattern having a plurality of pixel columns in which the pixels are arranged in a column direction (the pixel matrix receives from the data driver (352) the data lines in the column direction (see Fig.3A);

a plurality of data lines in the column direction (out of the data driver (352) are a plurality of data lines in the column direction,

a plurality of scanning lines in the row direction (out of the row driver (353) are a plurality of scanning lines in the row direction,

wherein the pixel each a light emitting element (EL element Fig.3B (303)),

x data lines out of the plurality of the data lines extended in each of the pixel columns (see Fig.3A, the data lines from the data driver (352)), a one scanning line out of the plurality of scanning lines extending in each row (see Fig.3a, where the scanning lines from the row driver (353)), comprising the steps of:

dividing one frame period into a plurality of sub-frame periods (one frame period has n subframe periods SF.sub.1, SF.sub.2, . . . , SF.sub.n (page 5, paragraph 0059)),

dividing each of the plural sub-frame periods into a writing period and a light emission period, or a writing period, a light emission period, and an erasure period (the address (write in) periods and sustain (turn on) periods are completely separated (a driving method in which the sustain (turn on) period begins after the address (write in) period of one pixel portion completely finishes in each subframe period), the proportion within one frame period occupied by the address (write in) period becomes large. Further, as shown in FIG. 15A, a period 1501 develops, in which write in and turn on cannot be performed in other rows, during a period in which the gate signal line of a certain row is selected within the address (write in) period. The duty ratio (the length proportion of the sustain (turn on) period within one frame period) is thus greatly reduced. Increasing the operational clock frequency is the only way to shorten the address (write in) period, and considering things such as the circuit operating margin, there are limits to making multiple gray scales (page 2, paragraph 0024)). Accordingly, the prior art teaches all the claimed limitations with the exception of providing selecting y scanning lines simultaneously by a scanning drivers whereas simultaneously supplying signals by the x data drivers to x pixels selected out of the plurality of pixels through the x data lines extending in each of the pixel columns.

However, Yashioka teaches the display unit 10' has 1000 scanning lines, and these scanning lines are divided into, for example, eight groups A to H. Hence, in each of the groups A to H, the scanning line is selected simultaneously, so that different data can be written simultaneously into the groups A to H (column 11, lines 34-39)).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the display selection as taught by Yoshioka in the display panel disclosed by Kimura because this would provide an image display method capable of enhancing the rate of period contributing to display within the period of one field, and obtaining a bright display image, and a device used in execution thereof (column 3, lines 19-23).

As for claim 20, Kimura et al. teach a driving method of a display device (an active EL display device is shown in FIGS. 13A and 13B. FIG. 13A is a schematic diagram of an entire circuit) that has a plurality of pixels arranged in a matrix pattern in a pixel portion (pixel Fig.3A (300) is arranged in a pixel matrix 351) , the matrix pattern having a plurality of pixel columns in which the pixels are arranged in a column direction (the pixel matrix receives from the data driver (352) the data lines in the column direction (see Fig.3A);

a plurality of data lines in the column direction (out of the data driver (352) are a plurality of data lines in the column direction,

a plurality of scanning lines in the row direction (out of the row driver (353) are a plurality of scanning lines in the row direction,

wherein the pixel each a light emitting element (EL element Fig.3B (303)),

x data lines out of the plurality of the data lines extended in each of the pixel columns (see Fig.3A, the data lines from the data driver (352)), a one scanning line out of the plurality of scanning lines extending in each row (see Fig.3a, where the scanning lines from the row driver (353)), comprising the steps of:

dividing one frame period into a plurality of sub-frame periods (one frame period has n subframe periods SF.sub.1, SF.sub.2, . . . , SF.sub.n (page 5, paragraph 0059)),

dividing each of the plural sub-frame periods into a writing period and a light emission period, or a writing period, a light emission period, and an erasure period (the address (write in) periods and sustain (turn on) periods are completely separated (a driving method in which the sustain (turn on) period begins after the address (write in) period of one pixel portion completely finishes in each subframe period), the proportion within one frame period occupied by the address (write in) period becomes large. Further, as shown in FIG. 15A, a period 1501 develops, in which write in and turn on cannot be performed in other rows, during a period in which the gate signal line of a certain row is selected within the address (write in) period. The duty ratio (the length proportion of the sustain (turn on) period within one frame period) is thus greatly reduced. Increasing the operational clock frequency is the only way to shorten the address (write in) period, and considering things such as the circuit operating margin, there are limits to making multiple gray scales (page 2, paragraph 0024)). Accordingly, the prior art teaches all the claimed limitations with the exception of providing selecting y scanning lines simultaneously by a scanning drivers whereas simultaneously supplying signals by the x data drivers to x pixels selected out of the plurality of pixels through the x data lines extending in each of the pixel columns.

However, Yashioka teaches the display unit 10' has 1000 scanning lines, and these scanning lines are divided into, for example, eight groups A to H. Hence, in each

of the groups A to H, the scanning line is selected simultaneously, so that different data can be written simultaneously into the groups A to H (column 11, lines 34-39)).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the display selection as taught by Yoshioka in the display panel disclosed by Kimura because this would provide an image display method capable of enhancing the rate of period contributing to display within the period of one field, and obtaining a bright display image, and a device used in execution thereof (column 3, lines 19-23).

Allowable Subject Matter

6. Claims 23-34 are allowed.

7. The following is an examiner's statement of reasons for allowance: the claimed invention is directed to a display device.

Independent claim 23 identifies a uniquely distinct feature "first data driver for supplying a video signal to the pixels which are arranged in first to m/2-th rows and in odd-numbered rows; a second data driver for supplying a video signal to the pixels which are arranged in first to m/2-th rows and in even-numbered rows; a third data driver for supplying a video signal to the pixels which are arranged in (m/2+1)-th to m-th rows and in odd-numbered rows; a fourth data driver for supplying a video signal to the pixels which are arranged in (m/2+1)-th to m-th h rows and in even-numbered rows".

Independent claim 24 identifies a uniquely distinct feature "a second driver for controlling the scanning line extending in the (m+1)-th row; a third driver for controlling

the scanning line extending in the (m+2)-th row; and a fourth driver for controlling the scanning line extending in the (m+3)-th row".

Independent claim 24 identifies a uniquely distinct feature "a first scanning driver for controlling the scanning lines extending in the first to m/4-th rows; a second scanning driver for controlling the scanning lines extending in the (m/4+1)-th row to m/2-th rows; a third scanning driver for controlling the scanning lines extending in the (m/2+1)-th row to 3xm/4-th row; a fourth scanning driver for controlling the scanning lines extending in the (3xm/4+1)-th row to m-th row".

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 2/10/2006

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER